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U.S. Patent & Trademark Office, U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <small>(Use as many sheets as necessary)</small>		Complete if Known	
		Application Number	10/765,301
		Filing Date	January 27, 2004
		First Named Inventor	Leslie, Terrence
		Group Art Unit	2815
		Examiner Name	Landau, Matthew
Sheet 1 of 1		Attorney Docket No: 303.860US1	

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
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<i>ml</i>		HERGENROTHER, J M., et al., "The vertical replacement-gate (VRG) MOSFET: a 50-nm vertical MOSFET with lithography-independent gate length", Bell Laboratories, Lucent Technologies, Murray Hill, 4pgs	<i>(NO DATE)</i>	✓
<i>ml</i>		ISA, "IBM claims speediest silicon transistor", http://www isa org/Template cfm?Section=Communities&template=/TaggedPage /DetailDisplay.cfm&ContentID=20445 , ISA - The Instrumentation, Systems and Automation Society,(November 4, 2002),2 pgs		
<i>ml</i>		LUCENT TECHNOLOGIES, "Revolutionary transistor design turns the silicon world on end", http://www.bell-labs.com/news/1999/november/15/1.html , Lucent Technologies, Bell Labs Innovations (1999),3 pgs		
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<i>ml</i>		NING, T H., "Why BiCMOS and SOI BiCMoS?", IBM, 0018-8646,(11.29.01),7 pgs		

EXAMINER

Matthew C. Johnson

DATE CONSIDERED

7/28/06

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached

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PTO/RB/004(10-01)
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<i>M</i>		GEPPERT, LINDA , "Triple Gate Double Play: Transistors with three gates and 3-D geometries will replace today's devices in a few years", <u>IEEE Spectrum</u> , (November 2002), 18		

EXAMINER	<i>Matthew P. Landau</i>	DATE CONSIDERED
		<i>7/28/06</i>

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Group Art Unit	2815
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